Abstract

Metallization arrangement for semiconductor structure and corresponding fabrication method

The present invention provides a metallization arrangement for a semiconductor structure (1) having a first substructure plane (M1), preferably a first metallization plane; a second metallization plane (M2) having a first and a second adjacent interconnect (LBA; LBB); a first intermediate dielectric (ILD1) for mutual electrical insulation of the first substructure plane (M1) and second metallization plane (M2); and via holes (V) filled with a conductive material (FM) in the intermediate dielectric (ILD1) for connecting the first substructure plane (M1) and second metallization plane (M2). A liner layer (L) made of a dielectric material is provided under the second metallization plane (M2), which liner layer is interrupted in the interspace (O) between the first and second adjacent interconnects (LBA; LBB) of the second metallization plane (M2). The invention likewise provides a corresponding fabrication method.

Figure 1h